In the Claims:

Please cancel claims 27 and 33.

Please amend claims 1, 8, 14, 20, 26, 30, and 32, as follows:

1. (Currently amended) A method for programming programmable elements of a plurality of memory devices, each memory device having at least a first and second programmable element thereon, the method comprising:

programming the first programmable element of a first memory device of the plurality of memory devices; and

programming the second programmable element of a second memory device of the plurality of memory devices, the programming of the first and second programmable elements overlapping at least for a period of time.

2. (Original) The method of claim 1 wherein the programming of the first and second programmable elements occur substantially concurrently.

3. (Original) The method of claim 1 wherein the programming of the first and second programmable elements occur substantially sequentially.

4. (Original) The method of claim 1 wherein programming of the first programmable element comprises:

providing bank and fuse addresses corresponding to the first programmable element;

latching the bank address;

latching the fuse address; and

initiating a programming event in response to latching the fuse address to program the first programmable element.

5. (Original) The method of claim 4 wherein providing the fuse address ceases prior to the completion of the programming event.

6. (Original) The method of claim 1 wherein programming of the first programmable element comprises:

providing a bank address corresponding to an antifuse bank in which the first programmable element is located;

providing a first load command to latch the bank address;

providing a fuse address corresponding to the first programmable element;

providing a second load command to latch the fuse address; and

initiating a programming event in response to latching the fuse address to program the first programmable element.

7. (Original) The method of claim 1 wherein the programmable element comprises an antifuse.

8. (Currently amended) A ~~The~~ method for programming programmable elements of a plurality of memory devices, comprising:

in a first memory device of the plurality of memory devices, latching a first address corresponding to a programmable element located at a first location on the memory devices;

initiating a programming event to program the programmable element in the first memory device located at the first location;

in a second memory device of the plurality of memory devices, latching a second address corresponding to a programmable element located at a second location on the memory devices; and

before the completion of the programming event for the programmable element in the first memory device, initiating a programming event to program the programmable element in the second memory device located at the second location.

9. (Original) The method of claim 8 wherein the programming events for the programmable elements in the first and second devices occurs substantially concurrently.

10. (Original) The method of claim 8 wherein the programming events for the programmable elements in the first and second devices occurs substantially sequentially.

11. (Original) The method of claim 8 wherein latching the first address comprises:

the address latch is a first address latch and providing a first load command to the first memory device to latch the bank address;

providing a fuse address corresponding to the programmable element located at the first location; and

providing a second load command to the first memory device to latch the fuse address.

12. (Original) The method of claim 11 wherein providing the fuse address corresponding to the programmable element located at the first location ceases prior to the completion of the programming event for the programmable element in the first memory device.

13. (Original) The method of claim 8 wherein the latching of the first address and the second address occur substantially simultaneously.

14. (Currently amended) A method for programming ~~an external tester to program~~ programmable elements of a plurality of memory devices, comprising:

commanding a first of the memory devices to latch a first address corresponding to a programmable element located at a first location on the memory devices;

commanding a second of the memory devices to latch a second address corresponding to a programmable element located at a second location on the memory devices; and

programming the programmable elements of the first and second of the memory devices substantially concurrently.

15. (Original) The method of claim 14 wherein the programming of the programmable elements of the first and second of the memory devices is initiated substantially simultaneously.

16. (Original) The method of claim 14 wherein the programming of the programmable elements of the first and second of the memory devices is initiated substantially sequentially.

17. (Original) The method of claim 14 wherein commanding the first and the second of the memory devices comprises simultaneously providing a load command to the first and second of the memory devices.

18. (Original) The method of claim 14 wherein commanding the first and the second of the memory devices comprises sequentially providing a load command to the first and second of the memory devices.

19. (Original) The method of claim 14, further comprising providing the first address and the second address to the first and second of the memory devices, respectively, substantially simultaneously.

20. (Currently amended) A method for programming ~~an external tester to program~~ antifuses of a plurality of memory devices, comprising:

providing to a first memory device of the plurality an address corresponding to a programmable element to be programmed in the first memory device;

providing a load command to the first memory device to latch the address;

providing to a second memory device of the plurality an address corresponding to a programmable element to be programmed in the second memory device; and

providing a load command to the second memory device to latch the address.

21. (Original) The method of claim 20 wherein providing a load command to the first memory device and providing a load command to the second memory device occur simultaneously.

22. (Original) The method of claim 20 wherein providing a load command to the first memory device and providing a load command to the second memory device occur sequentially.

23. (Original) The method of claim 20 wherein providing an address to the first memory device and providing an address to the second memory device occur simultaneously.

24. (Original) The method of claim 20 wherein providing an address to the first memory device and providing an address to the second memory device occur sequentially.

25. (Original) The method of claim 20 wherein providing an address to the first and second memory devices ceases prior to the completion of a antifuse programming event.

26. (Currently amended) A memory device having external address terminals and data terminals, and further having an array of memory with redundant memory to replace memory cells therein ~~in accordance with programmed programmable elements~~, the memory device comprising:

an antifuse bank address latch coupled to the external address terminals for latching an antifuse bank address applied to the external address terminals corresponding to a bank of antifuses including a programmable element to be programmed by a programming event;

an antifuse address latch coupled to the external address terminals for latching an antifuse address applied to the external address terminals corresponding to the programmable element to be programmed by the programming event;

logic circuitry coupled to the address latch and the data terminals, the logic circuitry receiving antifuse bank and antifuse address load commands applied to the data terminals and providing control signals to the antifuse bank address latch and antifuse address latch in response to receiving the antifuse bank and antifuse address load commands to cause the antifuse bank address latch and the antifuse address latch to latch the respective addresses applied to the external address terminals as the antifuse bank and antifuse address corresponding to the programmable element to be programmed, all respectively; and

programming circuitry coupled to the antifuse bank address latch and antifuse address latch and at least a portion of the programmable elements, the programming circuitry performing the programming event to program the programmable element corresponding to the latched antifuse bank and antifuse addresses.

27-29. (Cancelled)

30. (Currently amended) A memory device having external address terminals and an array of memory with redundant memory to replace memory cells therein ~~in accordance with programmed antifuses~~, the memory device comprising:

a bank address latch for latching a bank address corresponding to an antifuse bank in which an antifuse to be programmed by a programming event is located;

a fuse address latch for latching an antifuse address corresponding to the antifuse to be programmed by the programming event; and

logic circuitry coupled to the bank and fuse address latches, the logic circuitry receiving address load commands and providing control signals to the bank and fuse address latches in response thereto to cause the bank and fuse address latches to latch the ~~respective~~ bank and fuse addresses, respectively, applied to the external address terminals as the bank and fuse addresses corresponding to the antifuse ~~programmable element~~ to be programmed.

31. (Original) The memory device of claim 30, further comprising programming circuitry coupled to the bank and fuse address latches, the programming circuitry performing the programming event to program the antifuse corresponding to the latched bank and fuse addresses.

32. (Currently amended) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising:

external address terminals;

data terminals;

an array of memory with redundant memory to replace memory cells therein ~~in accordance with programmed programmable elements~~;

an antifuse bank address latch coupled to the external address terminals for latching an antifuse bank address applied to the external address terminals corresponding to a bank of antifuses including a programmable element to be programmed by a programming event;

an antifuse address latch coupled to the external address terminals for latching an antifuse address applied to the external address terminals corresponding to the programmable element to be programmed by the programming event;

logic circuitry coupled to the address latch and the data terminals, the logic circuitry receiving antifuse bank and antifuse address load commands applied to the data terminals and providing control signals to the antifuse bank address latch and antifuse address latch in response to receiving the antifuse bank and antifuse address load commands to cause the antifuse bank address latch and the antifuse address latch to latch the bank and antifuse ~~respective~~ addresses, respectively, applied to the external address terminals as the antifuse bank and antifuse address corresponding to the programmable element to be programmed, all respectively; and

programming circuitry coupled to the antifuse bank address latch and antifuse address latch and at least a portion of the programmable elements, the programming circuitry performing the programming event to program the programmable element corresponding to the latched antifuse bank and antifuse addresses.

33-35. (Cancelled)